REFERENCE SLOTS FOR SIGNAL TRACES

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Field of the Invention

[0001] The present invention relates to printed circuit board (PCB) design.

Background of Invention

[0002] Increasingly complex designs are resulting in challenges to designers of printed circuit boards. Printed circuit board designs are becoming more complex due to various factors. One factor making printed circuit board designs more complex is related to the increase in the density of integrated circuit devices (i.e. the amount of logic on integrated circuit devices) that are used as part of a printed circuit board assembly. As integrated circuits increase in density, the number of input/output (I/O) signals to those integrated circuits increases while trying to maintain similar footprints on the printed circuit board. Thus, printed circuit boards supporting these increasingly dense integrated circuits become more complex with respect to the increased number of signal traces they support.

Brief Description Of Drawings

[0003] Embodiments of the present invention will be described referencing the accompanying drawings in which like references denote similar elements, and in which:

[0004] FIGs. 1A and 1B illustrate a top view and a cross section view of a portion of a prior art printed circuit board design.

[0005] FIGs. 2A and 2B illustrate views of a printed circuit board design including a slot in the reference plane, in accordance with one embodiment.

[0006] FIG. 3 illustrates a top view of a portion of a printed circuit board utilizing reference slots, in accordance with one embodiment.

[0007] FIGs. 4A-4C illustrate cross sectional views of regions of the portion of a printed circuit board of FIG. 3.

[0008] FIG. 5 illustrates a stripline signal trace pair, in accordance with one embodiment.

[0009] FIG. 6 illustrates a printed circuit board assembly design utilizing an embodiment of the present invention.

[0010] FIG. 7 illustrates a system included a printed circuit board having reference slots, in accordance with one embodiment.

Detailed Description of the Embodiments

[0011] In the following detailed description, a novel method and apparatus for utilizing a reference slot (i.e., a slot in a reference plane) are disclosed In this description, mention is made to the accompanying drawings which form a part hereof wherein like numerals designate like parts throughout, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present invention. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims and their equivalents.

[0012] FIGs. 1A and 1B illustrate a top view and a cross section view of a portion of a prior art printed circuit board design. Illustrated in FIG. 1A are two signal traces **140 142** routed parallel to each other for the portion of the printed circuit board design. FIG. 1B illustrates a cross section of one region showing a signal layer **160**, a dielectric layer **170** and a reference plane **180**. The signal layer contains signal traces **140 142**. The reference plane **180** may be coupled to ground or some other reference voltage. The reference plan may provide a reference voltage for the printed circuit board design.

[0013] The signal traces originate in a breakout region **110**, i.e., from an area with connections **150 152** to a silicon device (not illustrated). For example, the connections **150 152** may be pads to connect a surface mount device to the printed circuit board. In the breakout region **110**, the traces **140 142** may each have a

certain thickness t_1 **112**. In addition the traces **140 142** may have distance d_1 **114** between each other. As the signal traces **140 142** leave the breakout region **110** and transition to a second region **120**, the trace thickness, t_2 **122**, increases and the distance, d_2 **124**, between traces increases. As signals **140 142** fanout to a third region **130**, the trace thickness t_3 **132** further increases as does the distance d_3 **134** between traces.

[0014] The increase in thickness of the signal traces may provide for, among other things, increased signal integrity in terms of reducing loss in signals transmitted on the signal traces. As the trace width increases in a new region, if the distance between the signals is not increased, the impedance of the traces in this new region may not match the impedance of the previous region. This may occur, for example, due to differential impedance between the signal traces. To provide for the ability to match impedances between regions, in this prior art design, the spacing between the signal traces is increased as the signal trace widths are increased.

[0015] However, the increased distance between the signal traces may reduce the ability to perform high density routing of signal traces on the printed circuit board. Since more space is necessary between the traces, the lower the total number of signals that may successfully be routed on the printed circuit board during layout, given the spacing rules for a printed circuit board technology. By reducing the spacing between signal traces on a circuit, it may be possible to increase the number of signals that can be successfully routed.

[0016] In addition, in a breakout region of a design, with trace widths reduced to a value that still provides enough signal integrity and a desired target impedance, there

is a limit to the minimum separation on signals in the breakout region. This in turn limits the density of pins on a device connected to the printed circuit board, e.g., at pads **150 152**. Thus, to increase the number of input/output signals, and thus the number of pins, on a device, the device package increases in size. This may be undesirable for a number of reasons.

[0017] FIG. 2A illustrates a cross sectional view of a printed circuit board design including a slot in the reference plane, in accordance with one embodiment. Illustrated are signal trace pair **290** in a signal layer **260**. Also illustrated is a dielectric layer **270** and reference plane **280**. In one embodiment, the signal trace pair **290** may carry differential signal pairs. As such, the traces may originate at approximately the same location on a printed circuit board and terminate at approximately the same location on a printed circuit board. For example, a differential signal pair may source from closely spaced output pins of a processor and terminate at closely space input pins of a networking device. To improve common mode noise rejection between signals carried on the differential signals carry to the signal trace pair **290**, the signal traces may be routed on the printed circuit board substantially parallel to each other from source to termination.

[0018] As illustrated, the design includes a slot **285** in the reference plane **280** (i.e., a reference slot) that runs substantially parallel to the signal trace pair **290** and is centered between the signal trace pair **290**. FIG. 2B illustrates a top level view of a printed circuit board design illustrating the signal trace pair **290** as well as the slot (hidden) which runs substantially parallel to the signal traces but along an opposite side of dielectric **270**. Signal trace pair **290** comprises two substantially parallel

signal traces **292 294**. The two substantially parallel signal traces **292 294** are separated by a trace width TW **296**. The slot width, SW **286**, in the reference plane is also illustrated. While the embodiment has illustrated the reference slot as being centered between the signal trace pair, in alternative embodiments the reference slot may be off center.

[0019] References slot **285** advantageously provides for reduced impedance for signals traveling on signal traces **290**. For a desired impedance on signal traces **290** with a given trace width, there is a limit to the distance between signal traces. However, by utilizing a reference slot parallel to the signal traces, the impedance in the signal traces can be reduced. Thus, signal traces that are routed in high density areas of a printed circuit board may be laid-out closed together, while keeping the same impedance as traces further apart but with no reference slot. The width of the reference slot may determine the effect of the impedance change on the signal traces. A wider slot width may result in a further decreased impedance.

[0020] FIG. 3 illustrates a top view of a portion of a printed circuit board **300** utilizing reference slots, in accordance with one embodiment. Illustrated are multiple regions **310 320 330** through which signal traces **342 344** pass. As the signal traces **342 344** move further away from breakout region **310**, e.g. from a region with connections **352 354** to a silicon device (not illustrated), the trace width of the signal traces **342 344** increases. Thus, in a second region **320** the trace width, w2 **322**, is greater than in the breakout region **310**. In a fanout region **330**, the trace width, w3 **332**, is greater than in the second region **320**.

[0021] In comparison to the prior art design described in connection with FIG. 1, in the embodiment illustrated in FIG. 3, when the traces increase in thickness as they pass from region to region, the spacing between the traces **314** may, in one embodiment, remain substantially constant. Utilizing reference slots, impedance matching can be obtained between regions without the need to change the spacing between traces. This may result in the ability to have more dense signal trace layout over a printed circuit board.

[0022] FIGs. 4A-4C illustrates cross sectional views of regions of the portion of a printed circuit board of FIG. 3. FIGs 4A, 4B and 4C correspond to cross sectional views of regions **310, 320,** and **330**, respectively. Each cross section illustrates signal traces **342 344** which change width as the regions change. Also illustrated is dielectric **360** separating a signal layer, containing traces **342 344**, from reference plane **470**. By adaptively changing the width of slots in the reference plane, the impedance associated with corresponding signal traces may be modified. For example, in the embodiment illustrated, signal traces **342 344** have a trace width, tw1 **312**, in a first region **310**. To achieve a particular impedance, for example 80 ohms, a corresponding slot with width w1 **414** is placed in the reference plane **470**. The determination of a slot width to provide a particular impedance may be empirically ascertained. The signal traces **342 344** have a different width, tw2 **322**, in a second region **320**. In the embodiment illustrated, as a result of the different width, tw2 **322**, a corresponding slot with width w2 **424** is placed in the reference plane **470**. This slot width **424** is chosen to result in the impedance in the signal traces **342 344** matching the impedance of the signal traces in the first region **310**, i.e., 80 ohms.

Similarly, the slot width in the fanout region of the portion of the printed circuit board is chosen to result in a matched impedance of 80 ohms in the fanout region.

[0023] FIG. 5 illustrates a stripline signal trace pair, in accordance with one embodiment. The stripline signal trace pair **542 544** (e.g. a signal trace pair routed in one of the inner layers) is "between" two reference planes **580 582**. That is, as illustrated, a first reference plane **582** is above the stripline signal trace pair **542 544** and a second reference plane **580** is below the stripline signal trace pair **542 544**. In the embodiment illustrated, both reference planes **580 582** may contain reference slots **510 512** which run parallel to the signal traces **542 544**. In the illustrated embodiment, both reference planes **580 582** have slots **510 512** of equal width **590** to facilitate reduction in the impedance in signal trace pair **542 544**. In another embodiment in a stripline design, only one of the reference planes contains a slot. In yet another embodiment, each reference plane contains a slot, however the two slots have different widths.

[0024] FIG. 6 illustrates a printed circuit board assembly **600** utilizing an embodiment of the present invention. For the embodiment, printed circuit board assembly **600** includes printed circuit board **620**, includes buses **614a-614b**, processor **602**, non-volatile memory **604**, memory **606**, bus bridge **608**, interface to persistent storage **610**, interface to networking equipment **614** and interfaces to other I/O devices **612** coupled to each other as shown.

[0025] Buses **614a-614b** comprise a number of signal traces for carrying signals between various devices on the printed circuit board as illustrated. In the embodiment illustrated, a top layer of the printed circuit board **620** contains microstrip

traces on a dielectric material. The dielectric material may separate the microstrip traces from a reference plane (not illustrated). Reference slots may be utilized in the reference plane for one or more signal trace pairs to advantageously modify the impedance of signal using the signal trace pairs.

[0026] FIG. 7 illustrates a system **700** included a printed circuit board having reference slots, in accordance with one embodiment. System **700** contains a printed circuit board **710**. The printed circuit board **710** contains reference slots associated with signal trace pairs, in accordance with one embodiment of the present invention. In addition, the system **700** comprises a number of peripheral devices coupled to the circuit board **710** via various interfaces **712-716**. For example, networking equipment **726** may interface to circuit board **710** via a Universal Serial Bus **716**. Persistent storage **722** may interface to circuit board **710** via an Parallel Advanced Technology Attachment (UATA-100) interface.

[0027] Although specific embodiments have been illustrated and described herein for purposes of description of the preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent implementations calculated to achieve the same purposes may be substituted for the specific embodiment shown and described without departing from the scope of the present invention. For example, the above description may apply to other apparatus such as integrated circuits. Those with skill in the art will readily appreciate that the present invention may be implemented in a very wide variety of embodiments. This application is intended to cover any adaptations or variations of the embodiments

discussed herein. Therefore, it is manifestly intended that this invention be limited only by the claims and the equivalents thereof.